SYNERGY SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL ENGINEERING

Discipline: Computer science Engineering	Semester: - 3rdsem CSE	Name of the teaching faculty: -PRAJNAPARAMITA KABI		
Subject: - Digital electronics Lab	No. of Days/week class Allotted: 4	No. of weeks: -15 SESSION-2026-27 WINTER Starting date- 1/7/2026 Ending date 5/11/2026		
No. of week	No. of lab class	Topic to be Taught	DATE OF DELOVERY G1	G2
1ST	1st	To verify the truth tables for all logic gates: NOT, OR, using CMOS Logic gates and TTL Logic Gates		
	2nd	To verify the truth tables for all logic gates: AND, NAND, using CMOS Logic gates and TTL Logic Gates		
2ND	1st	To verify the truth tables for all logic gates: XOR, XNOR using CMOS Logic gates and TTL Logic Gates		
	2nd	Implement and realize Boolean Expressions with Logic Gates		
3RD	1st	Implement and realize Boolean Expressions with Logic Gates		
	2nd	Implement and realize Boolean Expressions with Logic Gates		
4TH	1st	Implement Half Adder, Full Adder, using ICs		
	2nd	Implement Half Subtractor, using ICs		
5TH	1st	Implement Full Subtractor using ICs		
	2nd	Implement parallel full-adder using ICs.		
6TH	1st	Implement serial full-adder using ICs.		
	2nd	Implement serial full-adder using ICs.		
7TH	1st	Design and development of multiplexer using multiplexer ICs		
	2nd	Design and development of De-multiplexer using multiplexer ICs		
8TH	1st	Design and development of De-multiplexer using multiplexer ICs		
	2nd	Verification of the function of SR, Flip Flop.		
9TH	1st	Verification of the function of D, Flip Flop.		
	2nd	Verification of the function of JK, Flip Flop.		
10TH	1st	Verification of the function of T Flip Flop.		
	2nd	Design controlled shift registers.		
11TH	1st	Design controlled shift registers.		
	2nd	Design controlled shift registers.		
12TH	1st	Construct a Single Digit Decade Counter (0-9) with a 7-segment display.		
	2nd	Construct a Single Digit Decade Counter (0-9) with a 7-segment display.		
13TH	1st	Construct a Single Digit Decade Counter (0-9) with a 7-segment display.		
	2nd	Construct a Single Digit Decade Counter (0-9) with a 7-segment display.		
14TH	1st	To design a programmable Up-Down Counter with a 7-segment display		
	2nd	To design a programmable Up-Down Counter with a 7-segment display		
15TH	1st	To design a programmable Up-Down Counter with a 7-segment display		
	2nd	To design a programmable Up-Down Counter with a 7-segment display		

Prepared by 2/6/26

HOD EE 5/6/26

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